SHARIEF MEGEED

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SUMMARY

Experienced **software**, **hardware** and **digital design e**ngineer with a proven record in architecture, development, verification, and lab evaluation. Expertise include **FPGA/ASIC** in the fields of telecommunications, wireless RF, and video. In addition, experienced technical **project manager (PMP Certified)** engineer with a proven record in leadership, scheduling, and resource allocation.

TECHNICAL SKILLS

Languages:	Verilog, VHDL, Perl, C/C++/C#, Java
Sim/Debug:	MTI Modelsim, Modelsim, Signalscan, Cadence Ncsim, Debussy, Undertow, Synopsys, Realintent, Telecom Workbench, Cadence Verilog Sim, Visual Elite
Synthesis:	Synopsys Design Compiler, Design Analyzer, Synplify, Leonardo Spectrum, ORCA Foundry, Exemplar, Altera Quartus, Actel Designer, Cadence Buildgates, Xilinx ISE and Vivado
Standards:	Telecordia GR-253, ITU-T (G703, G707, G742, G753, G751, G.7042, G.803, G984.3, G987.3) SONET/SDH
Protocols:	GPON, PCIe, DDR3, SONET/SDH, ATM, ETHERNET, VIDEO (NTSC etc)
Lab Equipment:	Logic Analyzer, Oscilloscope, IXIA Ethernet tester

EXPERIENCE

Spirent Communications, Eatontown, NJ **2011 – Present**

Program Manager / Product Development Staff Engineer – Project Team Lead

Next Generation Network Emulator – Elevate (C, C++)

- Design and code firmware, DLL and test tool for Freescale BSC9131 processor. Functionality included Linux drivers to control the system and DSP core.

Next Generation Network Emulator – MercuryHD (Verilog)

- Lead integration effort of four modules for LTE Network Emulator.
- Manage schedule and resources for Software framework and FPGA design and verification.
- Manage architecture and design efforts of RF services and two Xilinx Virtex 7 FPGAs

Next Generation Network Emulator – Terminator (C#, C++, C)

- Lead integration effort of four modules for Network Emulator.
- Lead a team to design, implement and code two controller boards. Design included board level design, test, and code FPGA uBlaze and TI Microprocessor using C.
- Implement C# coding of Instrument Control Module Driver Host.
- Debug and add features to Instrument Control Module Driver using C++.
- Design verification test plan for RF services, Power testing, HALT/HASS testing and Thermal testing.
- Oversee scheduling and resource allocation for Instrument Control Module design and test efforts.
- Create Statement of Work, schedule and resource allocation for Instrument Control Board redesign.

FPGA design, quality and education advisor (Xilinx, VHDL, Verilog)

- Create Spirent FPGA design guidelines
- Create and hold educational FPGA training
- Determine and plan Xilinx training for team members.
- Coordinate Xilinx lunch and learn session for the Wireless Division
- Active member of the Spirent Quality Initiative

Program Manager – Elevate Platform

- Manage cross function team efforts from inception to completion of the Elevate Network Emulator Releases 1.01, 1.10, 1.15 and 1.20
- Manage both the hardware and software development teams along with Sales, Quality and Support teams to meet Product Manager's requested features and time line.
- Manage contract needs and operations timelines.

US Patent and Trademark Office, Alexandria, VA **2011 – 2011**

Patent Examiner

- Examine, reject and allow patent applications in the network security and cryptography art.
- Achieved 115% production reviewing patent applications. Earned eligibility for accelerated promotion.

Alphion, Princeton Junction, NJ **2007 – 2011**

FPGA Design Engineer

GPON Reach Extender Altera FPGA (Verilog)

- Architect and design GPON downstream bit aligner, downstream deframer, downstream TX and RX phy, I/O ring, FPGA top level, downstream top level, upstream top level, upstream bit aligner, microprocessor interface.
- Primary FPGA Altera designer. Created and placed I/O. Created timing constraints and insured FPGA met timing.
- Co-authored provisional patent "System and Method for Optical-Electrical-Optical Reach Extension in a Passive Optical Network"
- Co-authored paper "Frame-level OEO-Regenerating GPON Reach Extender"

Ethernet-GPON OLT Xilinx FPGA (Verilog)

- Take existing one PON FPGA and implement a two PON FPGA using Verilog.
- Debug verilog and fix AES encryption algorithm in GPON design.
- Reduce size of existing GPON FPGA to fit and meet speed requirements.
- Reduce AES encryption from four ciphers to two.
- Debug and fix major GPON downstream lockup issue, GPON downstream data lose issue, and GPON AES encryption data lose issue.
- Evaluate and stream line Xilinx XST synthesis flow.
- Maintain and fix downstream and register map test cases.

Ethernet-GPON OLT Actel CPLD(VHDL)

- Add LOS count logic for continuous and timed detection for GLCP and GLC2 PLDs
- Add slow LED blink logic for GLCP and GLC2 PLDs.

Tyco Electronics, M/A-COM, Morristown, NJ **2006 - 2007**

Principle Digital Design Engineer

GSM/EDGE Closed-Loop Transmitter - SPCM (Product Integration 2) ASIC/ Xilinx FPGA

- Lead verification engineer on Product Integration 2 ASIC/FPGA chip.
- Verified Verilog DigRF interface, EDGE Symbol Processing (8PSK modulation, pulse-shaping and up-sampling FIR filters, CORDIC), SPCM (Synchronization/Power Control/Calibration/Mask), Amplitude Processing, Phase Processing, Feedback Processing and Test Mux block.
- Designed and verified Amplitude Autogain Feedback block and Test RAMs in Verilog using the Cadence Ncsim environment.
- Implemented Xilinx module level timing analysis and synthesis on entire Product Integration 2 chip using ISE.

GSM/EDGE/CDMA Closed-Loop Transmitter – SPCM ASIC (DTX_TX_IC)

- Architected, designed, and synthesized digital portion of a dual Analog to Digital Converter (A2D) using verilog in the Modelsim simulator and Cadence Buildgates synthesizer.
- Architected, designed and converted FPGA closed-loop transmitter into the DTX_TX_IC ASIC using Verilog in the Cadence Ncsim environment.

Digital Down Converter (DDC) for AeroEnvironment contract

- Architected and created resource/gate estimates for a Digital Down Converter (DDC).

L-3 Communications, Camden, NJ **2004 - 2006**

Senior Member of Engineering Staff

Actel, Xilinx & Altera FPGAs

- Architect, Design and Test Xilinx FPGAs in a wide band multi-channel receiver. Features include DDR memory, FIR Filter, FFT, and Aurora cores.
- Architected avionic graphic processing system FPGA. Used the Altera Stratix FPGA with the Quartus II software. Used Synplicity for synthesis and NCSIM for simulation. The design included a PCI target and DDR SDRAM core.
- Assessed redesign of Common Controller board to a smaller Dual Common Controller. Features included PCI, TDM, HDLC, USB, and 10/100/1000 Ethernet.
- Reversed engineered six Actel PLDs. Created and simulated the VHDL code using Visual Elite, Simplicity, MTI and Actel Designer. Tested and debugged PLDs in lab using oscilloscope and logic analyzer.
- Debugged and fixed Common Controller switchover issue by modifying two Actel FPGAs.
- Assessed FPGA size and cost for MIL-STD-1397E and 1553.

- Mentored college new hire in making fixes to an Altera FPGA.
- Reviewed and fixed L-3 CMMI Electrical Engineering Process.
- Technically reviewed the STE HIC Xilinx FPGA.
- Created company FPGA/PLD review checklist.
- Created a VHDL training class for the company.

Agere Systems (formerly Lucent Microelectronics), Allentown, PA **1996 - 2004**

Design/Verification Engineer – Mapper Design Group

Datamapper, Ultramapper, & Supermapper (SONET Mapper and Framer) ASICs

- Using Verilog/VHDL, designed & verified SPEMPR and LO VT Terminator blocks.
- Using Verilog, designed and verified Poisson & Bursty Algorithm.
- Worked on architecting Datamapper SONET/SDH front end from existing TADM IP.
- Verified using Synopsys TWB the LOVCAG portion of the Datamapper ASIC.
- Using VHDL, designed and verified E3 and Pointer Processor capability of the SPEMAPPER.
- Verified using Synopsys TWB the DS3DJA, MPU, E13, Digital Cross Connect and TOP level for the Ultramapper ASIC.
- Architected and designed FPGA to test jitter issue for Supermapper.
- Administrated Synchronicity's ProjectSync and DesignSync.

Applications Engineer – Broadband Access Group

ORCA FPGA/FPSC, Echo Canceller, Supermapper ASICs

- Designed and verified using Verilog the Serial Multiplexed Interface for the Supermapper.
- Supported FPGA, FPSC, Echo Canceller, Supermapper, and several other PDH products.
- Provided apps support for the Mid-USA region, Canada, Europe, New England regions.
- Provided sales, training and technical support to customers.
- Provided Application support for the STARM product development team.
- Wrote application notes, along with many other documents.
- Debugged and fixed the M12 FPGA for a Tier I customer.
- Recreated and reorganized ORCA Foundry Documentation.
- Designed the ORCA 3L evaluation board.

FPGA Technical Support Engineer

ORCA FPGAs

- Delivered excellent support by consistently solving over 90% of all customer issues within 24 hrs.
- Gained valuable applications experience by working on key customer designs in support of our short-handed applications group.
- Generated a number of technical application notes and answers to frequently asked questions.
- Defined and created a documentation wrapper for ORCA Foundry 9.2 and 9.35 which greatly facilitates searching the documents.
- Created and maintained the Quicklinks internal web site.

EDUCATION AND DEVELOPMENT

PMP – Project Management Professional Certification 2013
M.S., Computer Engineering, Lehigh University, Bethlehem, PA 2000
B.S., Electrical Engineering with Computer Option, Rutgers University, Piscataway, NJ 1996

Synopsys Chip Synthesis workshops
VHDL/VERILOG
Telecommunication Essentials
HSI Designer
Altera Quartus
System Verilog
SONET/SDH
Verisity
Synopsys: PCI Bus Protocol
Behavioral Synthesis
Mentor Graphics
PMP (Project Management) Classes

OTHERS

- US Citizen
- Highest Held - Top Secret – SCI w/ DOD

Sharief Megeed

- Franklin Township, NJ, USA
- NJ, USA

Contact Information

- megeed@gmail.com (Preferred)
- 7329103617 (Preferred)

Work History

Languages

- Arabic,

Skills

- **project management** | 4yrs | 2015
- **verilog** | 15yrs | 2014
- **vhdl** | 15yrs | 2014
- **architecture** | 2011
- **cadence** | 2011
- **engineering** | 2011
- **gsm** | 2011
- **java** | 2011
- **lotus notes** | 2011
- **network security** | 2011
- **perl** | 2011
- **technical support** | 2011
- **asic** | 4yrs | 2004
- **sonet** | 2004
- **altera** | 0
- **debugging** | 0
- **embedded systems** | 0
- **ethernet** | 0
- **fpga** | 0
- **hardware architecture** | 0
- **integrated circuit design** | 0

- **ip** | 0
- **microprocessors** | 0
- **modelsim** | 0
- **rtl design** | 0
- **signal processing** | 0
- **simulations** | 0
- **static timing analysis** | 0
- **wireless** | 0
- **xilinx** | 0
- **data extraction**
- **hardware**

Work Preferences

- Likely to Switch: Most Likely
- Willing to Relocate: No
- Travel Preference: Up to 50%
- Work Authorization:
    - US
- Work Documents:
    - US Citizenship
- Desired Hourly Rate: 70+ (USD)
- Desired Salary: 125000+ (USD)
- Security Clearance: No
- Third Party: No
- Employment Type:
    - Full-time

Profile Sources

- YouTube: https://www.youtube.com/channel/UCCZEhKPmAQ6zIjgpntq4QAQ
- Facebook: http://www.facebook.com/megeed
- FourSquare: https://foursquare.com/user/4915875
- Twitter: https://twitter.com/smegeed
- YouTube: http://youtube.com/user/smegeed
- Linkedin: http://www.linkedin.com/in/megeed
- Dice: https://www.dice.com/employer/talent/profile/76b83628855c9ff2fd2d384b92c21d3e8b8bde9a