Shaurya Haridas

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https://github.com/Shaurya14	<u>40894</u>	
Education		
 Master of Science in Ele 	ectrical Engineering, Syracuse University, USA N	May 2020
Bachelor of Engineering	g in Electronics, Mumbai University, India N	May 2017
Technical Skills		
Languages	C, C++, Python, Verilog, Perl	
Frameworks and Librari		
Tools	Visual Studio, VS Code, TFS, GIT, Source Control, GitHub, MATLAB, AutoCAD, P-SPICE,	
10013	H-SPICE, e-plan, Synopsys Tools (Design Vision, Tetramax, Formality), NuSVM, Intel (Altera), ModelSim, Keil u-Vision, Xilinx Vivado	(Quartus,
Academic Projects		
Design and Implement of NALU (Python 3, TensorFlow, NPL) Ma		/lay 2020
	ral Arithmetic Logic Units to learn to multiply all the numbers in an array in Python using Nu	-
• Used tanh and satur	rated sigmoid for implementation.	
Used training data s	set containing 50000 arrays of size 3, 4 and 5.	
Verification of synchr	ronous FIFO (SystemVerilog Assertions)	Apr 2020
 Designed and Verifi 	fied FIFO for various conditions using a testbench.	
 Checked conditions 	s such as Empty to Full, Full to Empty, Read when Full and Write when Empty.	
Implementation of He	Hopfield Network (Python, NumPy)	Feb 2020
 Implemented and to 	trained Hopfield networks for patterns vectors in {0,1} ⁸ which are represented in NumPy library.	
 Wrote code for lear 	Irn, update and energy functions to implement Hopfield Network.	
	plemented energies as to strain the Hopfield network.	
		Oct 2019
	ficiently sort thousands of lines of data in a telephone records and return required outputs.	
	tions to perform different tasks such as calling and sorting the data.	
Object Detection using Haar Cascade (Python 3, OpenCV, Linux)		Feb 2019
	predeveloped cascades for detecting face and eyes in Python and Git.	
	emented an 8 – stage Haar Cascade to detect an object (Sports Shoes) using OpenCV.	
	the OpenCV directory.	
	an Android phone to as camera input.	
• Designed a BIST to out of random gener	-Test Tool (Verilog, ModelSim, Tetramax) Nool in Verilog, consisting of a PRPG, MISR and Controller. Designed tool so it creates a golden erated binary codes and then checks if a particular circuit produces the same results. Ind Tetramax for synthesis of the design and testing.	Nov 2018 signature
	r ALU using ATPG for comparison.	
Work Experience Experi		
	eveloping and upgrading windows-based application. Extremely proficient in writing, analyz	zing, and
	pred procedures and functions.	0,
	ted business value added services to reduce the effort and increase the productivity.	
	g and experience in Software Development Life Cycle (SDLC) and Agile Methodology.	
Intern Syracuse Uni		Present
	ent hardware algorithms for VLSI CAD tools in C++.	
	for routing and placement of digital VLSI design.	
-	nent 16-bit RISC based CPU with x86 architecture in Verilog.	
	TAL Manufacturing Solutions (TATA), Pune Jan 2018 – J	un 2018
	, Controllers, micro controllers and modified electrical drawings to newer versions in e-plan and A	utoCAD.
• Reduced the time pe	per drawing for 2 days to 1 day.	
	pplications of the electrical drawings.	
I round internet to get	rat tham up and minning in two weaks dumng my tinal month at the company	

• Trained interns to get them up and running in two weeks during my final month at the company.