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27th October 1994, India

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SUMMARY

Electrical Engineering Graduate with expertise in Embedded Software/Firmware Development, Computer Architecture and with great deal of exposure in Digital design, Verification and Validation. Possess 2.5+ years of overall experience in Software Industry. Currently Looking for Full Time roles starting from June 2021.

EDUCATION

Master of Science in Electrical Engineering — **8/2019 – 8/2021**
University of Texas At Arlington, Texas. — **GPA – 3.9**
Bachelor of Engineering in Electronics and Communication — **7/2012 – 6/2016**
Visvesvaraya Technological University, Belgaum, India. — **GPA 3.3**

TECHNICAL SKILLS

Programming Languages:	C, C++, Assembly, Perl, Python, Verilog.
Dev Tools:	CCStudio, STM32Cube IDE/Mx, GHS Multi, MATLAB, Simulink, GNU Toolchain (GCC,G++,MAKE,GDB), OpenOCD, SEGGER SystemView, Wireshark, Quartus Prime 18.1, Signal Tap Logic Analyzer, ModelSim, Waveform.
Peripherals and Protocols:	UART, SPI, ADC, DAC, GPIO, EEPROM, Ethernet, I2C(Theory Only), Timers, PWM, DHCP, UDP, TCP/IP, ARP, ICMP,MQTT.
Utility Tools	MS Office, Share LaTeX, GIT, SharePoint, Jenkins, Jira, FileZilla, Putty, HP QC.
Boards and Debuggers:	Intel 8051, Renesas R-Car M3 SOC, TM4c123GH6PM (Cortex M Series), STM32F446RE,De1SoC, ENC28J60, JTAG and ST-Link V2 (SWV), Oscilloscope, Logic Analyzer, Signal generator, Spectrum Analyzer.
OS:	FreeRTOS, IntegrityRTOS , Windows, Linux (Embedded / Ubuntu Distro)

WORK EXPERIENCE

Tech Mahindra — **October 2016- July 2019**
Software Engineer — Bangalore, India.

- Designed and developed solutions using Perl/python and shell scripting to automate manual tasks in Pre-Production Environment of BT-Ecommerce Portal. Solutions were well documented version controlled and maintained in Common SharePoint Repository.
- Worked as a Solaris Administrator, responsible for patching up pre-production environments with latest Solaris patches, was briefly involved in migration of servers to Linux.
- Set up a Testing framework for BSP testing of Renesas R-Car M3 SoC using Multi IDE, Jenkins, Jira, and BASH Scripting.
- Worked in an agile environment to perform testing of GPIO module i.e. to check the software state and outputs to match as per the functional requirements. Test cases were written using CUnit and build was performed using MAKE tool.

ACADEMIC PROJECTS

Low-Cost Programmable Pulse Generator — **Sept 2019 – Dec 2019**

- Built a very lost cost system using TM4C123GH6PMI microcontroller (cortex m4f core) with two channels each capable of generating both DC and Analog Sine, Square, Sawtooth, Triangle waveforms up to frequencies 60Mhz 10v peak-peak with added functionality to store previous data and display output.
- Project had a command line interface (using UART) capable of providing measurement data to the User.

DHCP and TCP State Machine Implementation on TM4C123GXL board — **May 2020-June 2020**

- Implemented DHCP client-side state machine which support user interface commands to request for release and refresh of the current assigned IP address and disabling of the DHCP for usage of Static IP.
- A TCP state machine was also designed to implement server functionality with support for one socket. A simple TELNET Server was implemented.
- The project was built upon pre-provided Ethernet framework and device drivers, packet analysis was done using Wireshark.

Design of 32-bit RISC processor — **September 2020 - October 2020**

- Designing a 32-bit scalar RISC microprocessor with load-store architecture, a 4-stage pipeline and Pseudo Harvard architecture including the instruction and data memory interfaces, register interface, and the entire pipeline control logic with full resolution of all structural, control, and data hazards.
- Processor was designed to implement a self - developed 32 Bit Instruction Set Architecture with support for 30 instructions all 32 bits wide in length and good amount of logic re-usage for operations such as PUSH/POP.

Design of a Custom Real-Time Operating System (RTOS) on Cortex-M4 processor — **September 2020 – November 2020**

- The implementation has option to switch between preemptive/cooperative and Round Robin/Priority Scheduling during run time by a Shell User Interface.
- It was designed to support a maximum of 5 semaphores and 12 tasks (since SRAM on the board is just 32kiB) and kernel functions such as yield, sleep, wait, post, killing and restarting threads etc/-.
- A Shell interface was implemented to control and peek into the system using commands such as (Kill, Run, PS, IPCS, pidof etc/-) it was designed to look and perform like a Linux shell.

Design of UART IP Core and Linux Device Drivers on De1SoC Board — **September 2020 – November 2020**

- Designed and implemented UART IP module on a Cyclone V FPGA, capable of being controlled and configured from the hard processor subsystem over an Avalon memory-mapped interface. Implemented Linux kernel modules for the UART IP as part of design.
- The design and Implementation of UART IP was be done using Verilog HDL and using Intel's Quartus Prime 18.1 EDA toolchain. IP is being tested using the linux kernel module developed in C.