Peter A. Moyle, P.E.
1035 CR 102
Paige, Texas 78659
(512) 797-8145 pmoyle111@gmail.com
Hardware/Firmware Engineer

HIGHLIGHTS OF QUALIFICATIONS AND SPECIALIZATION

30+ successful years of combined experience in Low-level Software Development in C/ASM (numerous uC's and uP's), Embedded Controller/FPGA based Hardware Designs, Analog for signal conditioning, and Linear and Switch Power Supplies. Diagnostics/ATE System Development for board and chip-level debug and bring up. Verification for CPU's and SOC's.

Objective: Consulting contracts involving Silicon or board level bring-up, validation, verification, diagnostics, associated tools development, or test development. Hardware and/or firmware or RTL design.

Expert in the following fields:

- Diagnostic Development: memory test/bus test/signal integrity testing, board/memory/chip bring-up
- C, ASM, Verilog, Perl
- Hardware designs utilizing 8051, x86, ARM CPU's /FPGAS's/A/D's to implement control/monitoring/data acquisition schemes.
- Embedded firmware/hardware design using x86/x51/PPC/ARM, embedded Linux, RTOS, Bare Metal
- MPU internals - Cache, TLB, Memory Controller, Machine Check, and peripheral blocks.
- FPGA, CPLD RTL.
- Debugging at the hardware (board or RTL) and software levels
- RTL Verification/Design

PROFESSIONAL EXPERIENCE

2/20 – Current

Computer Task Group , Microprocessor Programmer

Contractor at IBM. From Feb to June porting C/Asm exerciser code from P9 or Linux OS to P10 bare metal. Also making modifications and writing some new routines to the Perl regression infrastructure. Balance of time spent on Triage team debugging failed regression tests written in Perl in a Linux/Unix environment.

11/15 – 2/20

Dell, Inc Parmer Ln., Austin, TX

Software Senior Principle Engineer, Diagnostics - Started as contractor implementing middleware for new battery analytics being implemented in upcoming batteries. Worked with chip vendor, Battery team, and BIOS team to vet the specs and implement the module. Then integrated into library and released to group developing the actual analytics. Was given a task of making a rev on the diagnostic driver and subsequently inherited driver development. Have released several new drivers and middleware libraries. Developed a comprehensive SMI test tool (SmiTest) that checked for SMI's supported, executed them and could report data in a vast number of ways. Tool was aimed at large audience, so it had 20 different command line switches depending on user's needs. All code in C/C++. Also developed a utility (DcsaTstApp) for testing at middleware level. These tools supported Dell data Vault group and BIOS as well as Validation and EC.
Since 9/2019 began working on OrCAD schematics for STM32 based keyboard led true color PWM driver for Alienware products. Also made second version using NXP LPC55S69. Also researched component electrical compatibility and produced Digikey BOM. Have contributed fulltime to this project.

06/2014 – 10/15

ARM, Inc Deerfield Beach, FL. (Formerly Sunrise Micro Devices, Inc. - Acquisition Completed 04/18/15)

SOC Verification Consultant – Wrote and ported C based directed tests and Verilog based checkers and RTL stimulators to help the company meet an SOC tape out schedule. Worked authoring/porting/debugging tests/test benches/firmware for 4 tape outs. SOC consisted of 2 Cortex M0/+ cores, Bluetooth Mod/DeMod/Digital interface, Power Control, Serial Wire Debugger (SWD), I2C, SPI, etc., and Dig Debug Mux blocks. Wrote and debugged tests at both RTL and gate level. Significant Test Bench Development in Verilog. Authored ROM monitor with interrupt driven packet interface in Kiel C and Perl host driver providing command line user interface and LabVIEW API. Worked on FPGA implementation using Vivado and ISE. Designed schematics and layout for SOC eval module that plugged to a Xilinx Zynq board. Brought up board and spun layout rev to fix bugs. Regressed/debugged tests on Xilinx board using ChipScope Pro and logic analyzer.

1/2011 – 2/2014
Hubbell Building Automation, Inc. Austin, TX
Electrical Engineer – Developed both hardware and firmware designs using ARM Cortex M3, MSP430, and CPLDs. Designs included both high volume sensor and controls for commercial lighting control and test interface boards for factory floor. Interfaces involved were SPI, USB, RS-485, I2C, A/D. Heavy firmware work and debugging bare metal C. Re-engineered firmware for 2 major projects: Occupancy Sensor and combination RS-485 and wireless Host/client network for distributed lighting control. Heavy, multilevel state machine design/debug. Diagnostics for Cortex internal ram and SPI and I2C connected flash and EEPROM respectively. Wrote boot loader over RS-485 for client Micros. Signal integrity validation for SPI, and long-haul RS-485. Designed RS-485 interface to run at 4.5Mbs and 2400 feet of CAT5e. Wrote DMA routines to burst out 32KB packets of random data on one end and to receive and generate interrupt when full to check on the other end. Also wrote Perl scripts for test and automated build.

5/2010 – 1/2011
Network Appliance, Inc (aka "NetApp") Pittsburgh, PA
Hardware Validation Engineer Contractor - Reviewing schematic and third-party C source diagnostics and evaluating for coverage and making modifications as necessary. Writing Perl scripts to automate testing and provide logging and program prom images in system. Wrote formal requirements doc covering Pentium based main complex, Mips based service processor and disk expander subsystem. Reproduced procedure for determining SP DDR2 clock delay settings performed by Asian ODM. Deployed Iometer and Perfmon suites.

11/2009 – 4/2010
Polycom, Inc. Austin, TX (2nd contract)
Initial contract to perform MIPS/embedded Linux based DIAGs/bring up suite for new platform. Project was then canceled due to Silicon availability issues. In the interim, two early goals were accomplished: configure and build new kernel and port and debug kernel hacks from a previous rev that were failing.

Was redirected to perform other tasks such as a utility to receive characters over Ethernet and stuff them into the Linux keyboard buffer. Researched companies' PowerPC UBOOT based loader to redesign fundamental issues that arisen out of evolutionary development.

Was redirected again to research schematics, create test plans and perform hardware bench level verification on all video conferencing models using Tek mixed signal oscilloscope. Scope was to verify, and hunt bugs related to resets and switching supply sequencing. Units each had nearly a dozen resets for CPU, DSP's and FPGA's and nearly 2 dozen switching supplies. Captured scope shots for the record and found one serious bug and root caused to firmware.

9/2009 - 10/2009
Polycom, Inc. (short term contract) **Austin, TX**
Aiding in debugging Flash drive failures. Developing an ATE system to cycle power and simulate a customer flash update cycle with data acquisition from glitch detection circuits and serial port spew parsing. Have written test plan, USB interface layer in Win32/C and main test + 2 libs Perl, interface wiring in OrCAD. Completed 10/26/2009 with high customer satisfaction

2/2009 - 9/2009 Cisc Systems, Round Rock, TX
Working on an as needed/temp/consulting basis. This is a startup with extremely constrained resources. Target is an ultra-miniature AMD Opteron based embedded PC. Duties date have been as follows:

1) OrCAD schematic and Allegro PCB design reviews and cost reduction engineering.
2) Bring up and debugging Rev A boards, found fundamental problems that I have isolated to switch mode power supply due to bad layout.
3) Correcting and/or streamlining MOSFET multi-power switching circuits

***6/2007 - 12/2008 Advanced Micro Devices, INC**. Austin, TX*
Contractor - Verification Engineer
Performed basic formal pre-silicon verification for a new low power small footprint x86-64 core and Northbridge. As this core was considerably different most work needed to be done from scratch. Many challenges were face with design architectural changes. Work spanned the following duties:

- Developed Test Plans and wrote new tests and ported existing tests for the following blocks:
  MCA (machine check architecture) – CPU Core
    - DC (data cache) , IC(instruction cache), FR (completer)
    - tests included cache data and tag array error injection, TLB and L2TLB error injection and synthesized multi-match scenarios.
  Northbridge Integration - Core + verified NB at full chip
  MCA - NB, DDR, Microcode
    -Development of x86-64 assembly language tests
      - porting and debugging existing assembly language tests
      - debugging Verilog RTL, System Verilog Checkers, and C/C++ Checkers and Model interface widgets
      - trained 2 Indian engineers on X86-64 assembly language and test development
      - Met or exceeded all goals, most goals were characterized as aggressive; e.g., task given to debug 1000 self-test fails in 2 months; when regression was run to determine performance, came in just under 1100

6/2004 - 5/2007 NEWISYS, INC. Austin, TX
Systems Software Development Engr.
Diagnostics group 6/04 – 6/06
Basic duties were to develop diagnostics, bring-up tools, and board bring-up for multi CPU/core server systems.

Server DDR Memory test - Re-architected an existing Linux memory test which previously had low coverage. Was able to leverage top level hooks, and bottom level driver skeleton and replaced heuristic tests with algorithms based on science of memory testing. Prior to executing plan, developed a comprehensive proposal discussing memory test types, implications for hardware specific interaction, and final specifying 3 algorithms and a strategy for execution that would bring the largest bang for the buck. All testing was done inside the driver. Top level was used to manage the testing progress. My effort also revealed latent BIOS and System Management bugs that I worked with teams to debug. Added March C, Random Address and Retention tests, and revamped discovery/mapping of bios northbridge settings reporting. Performed maintenance by adding support for rev C, E, and F AMD K8 CPU's.

Cache Loadable Diagnostics - (aka ICACHE DIAG's, later became known as JDIAGS)
Charged with responsibility to bring Instruction/Data cache loadable diagnostics for bring-up efforts to Newisys. I had been the principle engineer on this previously at AMD. AMD effort relied on use of AMD's hardware debug tool to load these diags, which imposed a variety of limitations. Seeing that Newisys had done some JTAG interface already, I realized this could be leveraged to create a standalone embedded JTAG diagnostics and debug tool. Collaborated with my team lead to leverage the use of the company's latest PPC based system management board, to become dual use as a test debug system. The system was dubbed "JDIAGS" and became part of a critical requirement for bring-up of the company's HORUS chip/T-REX platform bring-up. Put on a companywide demonstration of a 4P platform booting and testing DDR DIMM's on all 4 CPU's with no BIOS or hard drives installed. All code loaded via JTAG to configure chips and the execute memory test. Progress could be seen on an attached Linux terminal. Other noteworthy pieces of that project I completed were as follows:

Was assigned debugging a FLASH rom update utility in critical mode where factory line had to be shutdown because failure rate of flash attempts exceeded allowable limits. Debugged this in 2 days and found minuscule coding error that was leading to intermittent invalid erasure of parts. Previously, parts that failed were labeled bad and returned to the manufacturer. This became a major issue when entire lots started to fail.

Worked with Hardware teams on bring-up and debug of early system validation, test and debug.
Worked with Kernel team to provide debug support at chip level.

6/06 - 12/06 HORUS BIOS Group

Worked on BIOS defects and enhancements from the Jira defect pile, defects included both NB and SB defects as well as working with ASIC team member to debug FPGA that allowed LPC flash update from System Management.

12/06 - 5/07 Sustaining Group

Worked on customer priority driven defects in all areas of software/firmware support including BIOS, Kernel, System Management

Developed test/evaluation interface for Infineon TPM evaluation module. Hardware interface patching method to LPC bus and BIOS to configure and remap TPM chip from IO to MMIO.

Developed proposal for HW/SW design for 8-way JTAG tool with USB interface for HORUS 32 K8 core system

- project lead for this effort
- utilized 100 MIPS 8051 (Silicon Labs), 2 Xilinx FPGA's

3/1998 - 1/2004 ADVANCED MICRO DEVICES, INC., Austin, Texas

(hired as contractor through XXCAL, Inc. 1st 9 months/accepted perm position),
Senior Systems Software Development Engineer - Diagnostics Development Group
Software accomplishments have been mostly at the hardware level, directly controlling or configuring CPU or chipset registers.

- Last completed project:
  A DRAM DIMM form factor board that utilized an FPGA for error generation logic, and an 8051 uC w/ USB connection for control by a Widows GUI based PC. Architected the project idea and wrote proposal describing architecture and design. Helped with bring-up and debugging and participated in design/schematic/layout and code reviews.
  Purpose: to place errors on the DDR bus for validating memory test diagnostics and for testing robustness of ECC.
  Independently invented the idea and wrote white paper detailing hardware concept, and selling design to management. Authored host GUI software using VC6/Win32, and controller firmware using Keil 8051 C.

- part of K8 bring-up team - first byte of code ever executed on K8 was mine.
- part of K7 bring-up effort.
- Developed diagnostics and utilities for Multi-level cache subsystems; SDRAM/DDR, PCI, IDE and other Southbridge devices using extended DOS (flat 32), ROM and Linux. Wrote general utilities and specifically targeted diagnostics to help debug team root cause specific issues. Worked on a initial phases of a diagnostics operating system dubbed DiagOS; Wrote first cache test using this methodology as a proof of concept

- Projects, included a diagnostic for bring-up and diagnosing DOA DDR subsystems using code run entirely from the L1 instruction and data caches, allowing DDR bus to be tested with no other support from ROM or Southbridge required (featured an interface to the JTAG emulator system (aka HDT), which allowed emulator host to perform high-level tasks my ICACHE-based diagram on the fly.
  Featured a BIOS settings extractor program to MASM compatible equate file binary image compiler/locator to allow settings to be loaded into data cache ram from HDT menus. Software was able to configure 1 to 8 processors similar to MP BIOS but specialized to allow "pure" diagnostic environment.

Software diags included DDR and HT bus and memory characterization, stability, DOA motherboard diagnosis, and other early bring-up debugging capabilities.
Collaborated with Platform Validation team, designed and implemented an ATE system for cycling power
up to 4 motherboards (per test station), logging behavior for each cycle. Tests included hard and soft power cycling and reset cycling. Used to test power supply, BIOS, and reset circuitry stability. Used DOS based GUI and printer port interface board to all DUT's. Performed interface with validation testers to determine look and feel of operator GUI, and designed and executed all phases of development including hardware interface board schematic, program in C, and maintenance.

1986 - 1999 ADVANCED DESIGN SOLUTIONS, INC., Atlanta, Georgia
Principle Engineer, Owner
Directed operations wrote proposals, interfaced with customers managed up to five (5) technical employees.
Performed all schematic, layout FPGA designs, bring ups.
Oversaw design, development, consulting, marketing and customer support of a wide range of products for the instrumentation, controls, industrial, scientific and military markets.
Directed sales and consulting of hardware modules and software library with a premier product being a DOS-based C library for animated virtual instrument displays. (In direct competition to National Instruments LabVIEW)
Hardware products/designs consisted of analog signal conditioning circuits, mixed signal circuits and power control circuitry (PWM and linear), FPGA, CPLDs, uP's, uC's with primary business in ISA, VME, RS232/485/422, and proprietary serial and parallel uses.
Used numerous schematic/layout systems, including ORCAD for Windows. Over 100 designs were from single chip ultra-low power to multi-controller designs with 2000+ components.
For select project histories, see addendum at end.

1984 - 1985 PROCESS AUTOMATION, INC., Atlanta, Georgia
Systems Engineer
Designed, managed installation of SCADA systems for large industrial companies. PLC's, DCS, motor controls.

1983 - 1984 LANHAM MACHINERY COMPANY, INC*., Atlanta, Georgia*
Electrical Engineer
Participated in development of controls system for conveyors, gas fired burners and quasi-robotic devices.
Used a mixture of PLC and micro-processor- based controls, off the shelf industrial control modules.

1981 - 1983 SOUTHWIRE COMPANY, INC., Carrolton, Georgia
Electrical Project Engineer
Continuing of development of sophisticated automation, control, and instrumentation systems, bring up of complex panels built by sister company (SMD, Inc.) and a solution to a plethora of challenges from very large plant-wide controls and monitoring of thousands of real-time signals (SCADA).

EDUCATION:
Bachelor of Electrical Engineering 1981,
Georgia Institute of Technology, Atlanta, Georgia

Additional coursework in CS and EE topics 1989 -1994, ~100 hours, a few courses short of second degree in CS
Many seminars in memory testing methods, FPGAs/soft processors, PCI, HT, Signal Integrity

DESIGNATIONS:
P.E. (Electrical Engineering), exam passed 1987, State of Georgia
EIT Exam passed in 1981

ADDENDUM I

Tools Experience:

C Compilers:

- VC++ 10, 13, 15, 17
- Kiel C/ASM, IAR for Cortex M0-4
- GNU C/C++
- Watcom C/C++

Buses:

- VME, ISA, PCI, PCIX, PCIe, I2C, LPC, RS-232/422/485, SPI, USB, DDR, DDR2, HT, S2K/CCI, JTAG, SAS, FC, 10Ge, SATA, AHB/AXI4

Assemblers:

MASM, TASM, NASM, LINUX embedded ASM (GAS)
IAR Cortex ARM, ARM assembler, MSP430

Scripting:

Bash/Csh
Perl
Python - completed online course in 2010

Hardware Tools:

OrCAD schematic/Allegro
Xilinx ISE thru 14.7, Vivado 13.2, Xilinx Chip Scope
Segger JLink
AMD HDT - expert user
TEK scopes (TDS 5/6/700, 3000, 7000 series) and logic analyzers TLA 700
Lecroy PCIe Analyzer

Revision Controls/Bug Reporting:

SOS
SVN, CVS, Tortoise SVN, TFS
Jira
Bugzilla
Team Track
Test Director
Star Team
Source Safe
Agile

Verification Tools:

Verdi/Debussy
VCS
Cadence ncVerilog Incisive, SimVision, NCSim
ModelSim

Development Environments:

Win32/DOS
Linux/Bash/Csh
UBOOT

CPU's:
x86 - K6, K7, K8, Fusion, Pent II/III
8051
ARM Cortex M0, M0+, M3, M4, ARM5, ARM9
MSP430

FPGA:
Xilinx Spartan/Virtex/ZYNQ, XC95144, ISE, Vivado
Lattice Mach4, XO2
MicroSemi/Actel Smart Fusion
Alterra – attended development environment seminar

ADDENDUM II

Projects at Advanced Design Solutions, Inc. from 1992 - 1999
Some photo's, schematics, boards, or code printouts or project design samples could be supplied upon request.

1999 Applied Data Systems, Columbus, Maryland
Multi-DC motor control/user interface for piece of Vermeer heavy machinery.

Performed 2 iterations, 2nd major upgrade from first. Involved use of Spartan 40 FPGA for 5 PWM channels with direction control and uP interface, 3 DS87C520's, 64 opto-isolated DIO's, 16 opto-isolated AIO's, and much more. Very large design: consisted of 2 stackable boards CPU and IO) 8” x 12” each using over 2000 components; distributed 42 Amps to a dc motors.

1997 Telecommunication Systems, Inc., Tampa, Florida
Design/built Audio Monitor Panel (AMP) systems. System used for military command/control center voice channel communication management. Unit had 10 full duplex voice audio channels allowing use with 600ohm balanced or unbalanced equipment, such as radios and telecom switches. Consisted of four (4) main subparts.

1) Custom designed aluminum 9U rack. 2) 3U channel interface boards. Contained analog and digital circuitry for receiving/transmitting audio, mixing switching and AGC. 3) Back plane used 10-96 pin (VME style) connectors with active circuitry.

1997 Applied Data Systems, Columbus, Maryland
Designed a PCB layout for an optically isolated I/O add-on board for their SBC (Pixel Press). Essentially adapted the below design for Norden Systems to a different bus interface and form factor.

1996-1997 Northrop Grumman Norden Systems, Norwalk, Connecticut
Designed/built a distributed remote discrete I/O system. System consisted of intelligent VME host communicating on RS485 network to remote interface boxes located on 3 wire bus up to one-mile long. 1) VME adapter used dual port ram to map remote bits into read, write and status areas for main VME computer boards. 2) Remote boxes consisted of three (3) subparts A) design of compact NEMA 12 enclosure with integral power supply, card cage and back plane, B) design of new DS87C520-based single board computer (MCU520), C) design of bi-directional optically isolated I/O expansion boards. Unique design allowed inputs to produce logic 1 on range from 2 - 60 volts without extension resistors. Network firmware and a command interpreter were developed for both host and slave boards. Both boards had designed in, the ability to download new firmware revs from a PC's RS232 port.

1996 GEC Marconi Avionics, Norcross, Georgia
Provided three (3) efforts toward company's overall project completion. 1) Turnkey firmware design/coding/debug to allow 8051-based MCU31 to emulate flight recorder as test set component of project. 2) Provided consulting and tech support to company's project engineer to jump start firmware for main control component. 3) Provided consulting to travel on-site to another subcontractor, providing pilot interface panel, with GEC manager to determining reasons why this sub-project had been stalled for months. Contractor delivered working unit several weeks later.

1996 Quincy Compressor, Bay Minette, Alabama
Developed PC/DOS GUI/Application for remote monitoring, control and data logging via modem of companies embedded control system. Program written in ANSI C contained more than 15,000 lines of real-time code. System could remote log new data while displaying graphical charts of previously logged data.

1994 - 1996 Shonka Research Association, Marietta, Georgia
1996 Built second run of devices.
1995 Second phase, board was miniaturized, digital pots changed to NV type, capabilities for flash serial prom and ADC added
1994 Designed PC/DOS GUI using GIL and RS232 remote board using DS87C520 to provide PC-based remote calibration for nuclear radiation detector (industry standard RO-2 and RO-30. Unit consumed 30 uA when idle and 11ma during bursts of communication
1992 Provided consulting to determine source of NMI's in PC-based data acquisition system.

1994 Temco Engineering, Norcross, Georgia
Designed/prototyped a position sensor for use in a consistency meter. Output was 4-20 ma. Loop powered. Consumed less than 2ma. Featured FET oscillator, envelope detector and Burr Brown XTR103 for loop interface. Made novel use of 800uA current outputs provided by XTR103 to construct regulated split supplies for front end circuits.

1993 Intel-Fab 5, Chandler, Arizona
Designed/built an instrument to catch errors in high voltage triangle waves used in an ion implantation machine. System used mixed signal front end arbitrated by MCU31 SBC, featured auto calibration and reported via RS232.

1991, 1993 ITT Rayonier, Fernandina Beach, Florida
1993 Designed/built of 32 channel full duplex RS232 Y data switch w/ESD protection for plant floor communications.
1991 Designed/Built of intelligent box for operator alert/acknowledge from inventory control computer via RS232.

1992 - 2000 Colorado State University, Ft. Collins, Colorado
Development of electronics for the SSP atmospheric research program. Provided all levels of work toward this project from hardware design to PCB layout and firmware. Project history had spanned SSPI initial concept and design, SSP1A partial redesign and consolidation, SSP2major enhancement and miniaturization. System now consists of five (5) stackable boards, hi-speed micro-controller, 12 independent 16-bit A/Ds and 48 muxed 12-bit A/Ds. Enhanced Optical detector board design and layout.

1992 - 1994 Venus Gusmer, Kent, Washington
Development of a turnkey process control/monitoring system (SCADA) for injection molding of auto body parts. Consisted of PC/DOS-based real-time graphics and MCU31 embedded controller. Controller acquired data from 10 thermocouples, flow meter, pressure sensor and local keypad/LCD display and reported via continuous RS232 stream.

Peter Moyle

- Paige, TX, USA

Contact Information

- 253-p6o-oh7@mail.dice.com (Preferred)
- 5122900124 (Preferred)

Work History

Total Work Experience: 17 years

- **ARM/Sunrise Micro Devices**
  Jun 01, 2014 - Nov 01, 2015
- **Electrical Engineer | Hubbell Building Automation, Inc**
  Jan 01, 2011 - Feb 01, 2014 | Austin TX United States
- **Hardware Validation Engineer | Network Appliance, Inc**
  Jan 01, 2010 - Jan 01, 2010 | Pittsburgh PA United States
- **Consultant | Polycom, Inc**
  Jan 01, 2009 - Jan 01, 2010 | Austin TX United States
- **SOC Verification Contractor | AMD**
  Jan 01, 2007 - Jan 01, 2008 | Austin TX United States
- **Software Engineer | Sanmina SCI/New Isys**
  Jan 01, 2004 - Jan 01, 2007 | Austin TX United States

Skills

- **assembler** | 30yrs | 2020
- **c** | 30yrs | 2020
- **i2c** | 15yrs | 2020

- **electronics** | 11yrs | 2020
- **perl** | 11yrs | 2020
- **spi** | 11yrs | 2020
- **usb** | 8yrs | 2020
- **verilog** | 8yrs | 2020
- **xilinx vivado** | 1yrs | 2020
- **c++** | 2020
- **documentation** | 2020
- **embedded systems** | 2020
- **ddr** | 11yrs | 2019
- **schematic orcad** | 11yrs | 2019
- **xilinx ise** | 20yrs | 2015
- **dos** | 11yrs | 2015
- **simulation** | 10yrs | 2015
- **arm m0-4** | 4yrs | 2015
- **8051** | 30yrs | 2014
- **dxdesigner** | 3yrs | 2014
- **embedded software** | 0
- **linux** | 0
- **xilinx**
- **arm**
- **orcad**

Work Preferences

- Likely to Switch: Most Likely
- Willing to Relocate: No
- Travel Preference: Prefers No Travel
- Preferred Location:
    - Austin, TX, USA
- Work Authorization:
    - US
- Work Documents:
    - US Citizenship
- Desired Hourly Rate: 75+ (USD)
- Security Clearance: No
- Third Party: Yes
- Employment Type:
    - Contract - Corp-to-Corp
    - Contract - Independent

Profile Sources

- Dice: https://www.dice.com/employer/talent/profile/0361f6d86841020c89b400d49d1f459786a196e4