Thirumalaikannan Nithiyanandan

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EXPERIENCE

Instructional Student Assistant, San Jose State University, San Jose *Aug 2019 - May 2020*

- CMPE224 Digital Design and CMPE140 Computer Architecture and Design.
- Organized and guided activities for students, including assignments and labs for students on combinational and sequential logic theory and circuits, Verilog modeling of Finite State Machines and Advanced computer Architecture.
- Assisted and mentored students in Lab assignments based on Vivado HLS and Basys 3 FPGA.

In-plant Trainee, Bharat Electronics Limited, India *Nov 2016 - Dec 2016*

- Gained knowledge on Development and Engineering department that monitors the tank functions, processes including optical control system by Testing the machines like T92.
- Learned about the quality management and testing procedures for sensors and other electronic gadgets used in the system to run the machine in different terrains.

PROJECTS

Study of FPGA using Reduced Precision with System Verilog and Vivado HLS, SJSU

- Implemented Arria-10-like DSP block using system Verilog and compared Performance, power consumption and number of cycles and memory utilization with enhanced DSP block that supports lower precision multiplication using Vivado HLS in different FPGAs including Zync family, Stratix 10:9 cores.
- Analyzed Memory utilization, power, speed parameters graphically with different FPGAs from the same family.
- **HDL & Tools used**: System Verilog, Vivado HLS.

Hardware Design using Zynq-7000 in Vivado HLS, SJSU

- Created a simple Hardware Design Using the Zynq processor along with two GPIOs that control LED and switch, respectively, Implemented and tested the design.
- **HDL**: Vivado HLS, Xilinx ZYBO.

Verification of APB bridge that interfaces APB bus with other AMBA BUS protocols using UVM

- Designed a Verification Environment that takes the APB bridge as a master that translates any AMBA protocols to APB bus and observes the transactions driven by the driver and verifies with monitor component.
- Randomized to check all the cases in the design and generated urg report for the verification performed.
- **HDL & Tools used**: UVM, Synopsys VCS.

The Design and Verification of a Synchronous FIFO Using System Verilog based UVM

- Designed a synchronous FIFO using Verilog and verifying using UVM test bench environment that can communicate with each port that verifies the correct functionality of data write and data read at the expected time.
- **HDL & Tools used**: System Verilog, UVM, Synopsys VCS.

A Simple Spread Spectrum Correlator Using Verilog at 333 MHZ, SJSU

- Designed and implemented correlator that runs at 333 MHz, which can accept base band sample Clock and produce a correlation output using gold code and phase shift keying. **HDL & Tools used**: Verilog, Synopsys VCS.

Low Power LNA Design in 45nm CMOS Technology using Virtuoso, SJSU

- This project includes an introduction to the key factors of BLE, an overview of the RF circuit theory, and the LNA design parameters. Each section provides detailed information and background knowledge to design a BLE front-end circuit. The LNA circuit gave exceptionally low energy consumption and NF. Depending on different purposes of the application, the focus of the design can be chosen among power, gain, NF, and linearity.

Bit Movement Block on AHB Bus Protocol Using System Verilog, SJSU

- Designed a bit movement block that works with 32 bits read and write interface that can move data at any bit location on AHB bus as master and slave using synthesizable system Verilog.
- **HDL & Tools used**: System Verilog, Synopsys VCS.

EDUCATION

Master of Science, Electrical Engineering, *Aug 2018 - May 2020*
San Jose State University, San Jose, USA

Bachelor of Engineering, Electronics and Communication, *Aug 2014 - May 2018*
Sri Venkateswara College of Engineering, Tamil Nadu, India

Relevant Courses: Soc Design & Verification, Advanced Digital System Design & synthesis, ASIC CMOS Design, Advanced Computer Architecture, RFIC Design, Semiconductor Devices, Digital Design for AI & DSP, Microprocessor and Microcontroller, VLSI Design, Linear Integrated Circuits, Circuit theory, Digital Signal Processing.

SKILLS

Languages, HDLs and OS: Verilog, System Verilog, C/C++, python, Linux, UVM (Universal Verification Methodology), JAVA.

Bus Protocols, Relevant concepts and EDA tools: AMBA APB, AHB, PCI., Static Timing Analysis, Assertions, Functional Coverage, RISC and CISC, DDR, Design for Test, Logic Synthesis, UVM testbench Development., Synopsys VCS, Quartus prime, Mentor graphics Model Sim, Xilinx ISE/ Vivado HLS, Cadence Virtuoso, GTK wave., debugging, Digital circuit Design, RTL coding, schematic , Eclipse IDE, Spring Boot, Postman.